THE BELL SYSTEM TECHNICAL JOURNAL
Vol. 57, No. 1, January 1978
Printed in U.S.A.

Accurate Silicon Spacer Chips for an Optical-Fiber Cable Connector

By C. M. SCHROEDER

(Manuscript submitted July 1, 1977)

Assembled silicon array connectors have been fabricated with low splice loss. The silicon chips can be manufactured with submicrometer repeatability and accuracy. Improvements in chip thickness variations are anticipated which in turn should reduce the overall groove opening variations to a point where individual chip selection is not required.

I. INTRODUCTION

Low-loss multifiber splices have been obtained with the use of accurate silicon spacer chips. These spacer chips are used in a unique splicing technique developed by Bell Laboratories[1] and used in the Atlanta Fiberguide experiment. This multifiber cable splice is a stacked array consisting of two properly prepared cable connectors butted end to end.

A cable array connector is a laminate sandwich of silicon alignment chips with "V" grooves on both top and bottom surfaces interleaved with optical fibers epoxied to form a two-dimensional array (Fig. 1). A completed connector may consist of up to 144 optical fibers positioned by up to 13 alignment chips. Each fiber in the array must be positioned accurately to its counterpart in a mating array to obtain low splice loss. The transverse misalignment of the mating fibers should be no greater than one-tenth the core radius or typically 2.5 micrometers.[2,3] This can only be obtained with alignment chips having high dimensional accuracy with respect to thickness, groove geometry, and position.

The feasibility of the multifiber splice was shown with alignment chips manufactured of aluminum. The aluminum chip, however, could not be manufactured repeatedly with the high dimensional accuracies required. An improved chip was developed, that met the above goals, using (100) oriented silicon[4] and photolithographic techniques. This improved chip has demonstrated a significant reduction in the overall array splice loss.

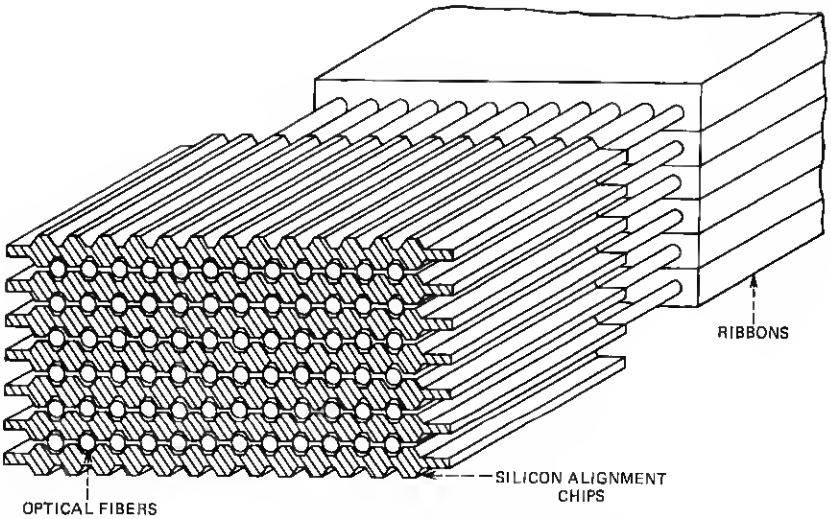

Fig. 1—Schematic of a multifiber array connector.

II. PHOTOLITHOGRAPHIC AND PROCESSING TECHNIQUES

The use of silicon for alignment chips offers several advantages. The material is readily available, it can be handled and processed relatively easily, and it can produce precise V grooves to photomask accuracy.

When a (100) surface slice of silicon covered by an oxide mask is submerged in a basic solution, the etch rate is much greater in the ⟨100⟩ direction than in the ⟨111⟩ direction (Fig. 2). This anisotropic etching of the silicon results in a precise V groove to an angle of 70.53° with the reaction self-stopping at the point where the (111) planes intersect. The groove opening is determined by the opening in the oxide mask. The (110) plane is used as a reference to align the photomask features parallel to the intersection of the (100), (111) planes.

The processing of the silicon first starts with the selection of a 5 cm diameter (100) surface oriented wafer polished on both surfaces to a thickness of 0.25 mm. Thickness variations and surface defects should

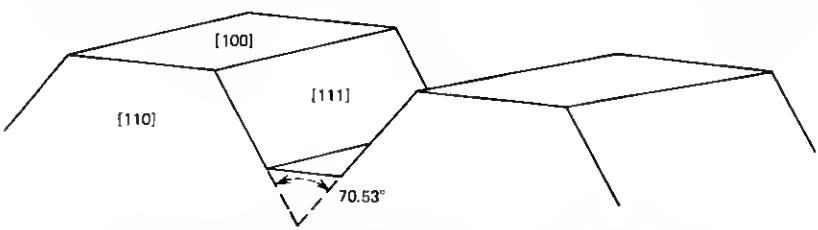

Fig. 2—Crystallographic planes used to manufacture alignment chips.

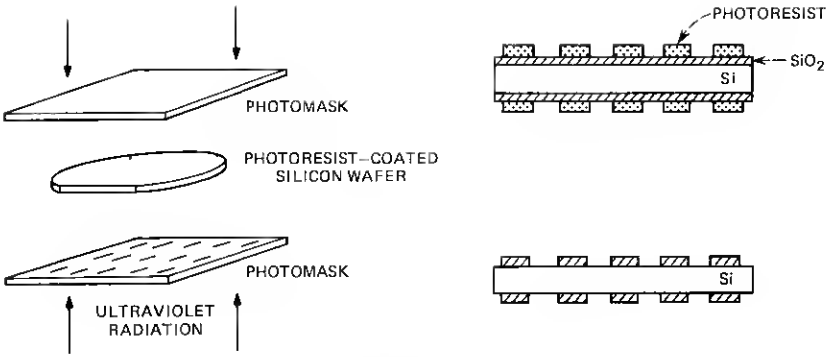

Fig. 3—Processing techniques.

be minimized for best results. The wafer is cleaned, then placed into a tube furnace for a 1-micrometer oxide growth. The wafer is then coated on both surfaces with a positive photoresist, placed between two prealigned photomasks and exposed to ultraviolet radiation (Fig. 3). The exposed wafer is removed, then developed leaving open windows of silicon oxide which are in turn etched in a buffered hydrofluoric acid solution. The remaining photoresist is removed leaving a silicon wafer covered by an oxide mask which is then placed into a potassium hydroxide solution for preferential etching[5]. A cross section of a typical silicon alignment chip is shown in Fig. 4.

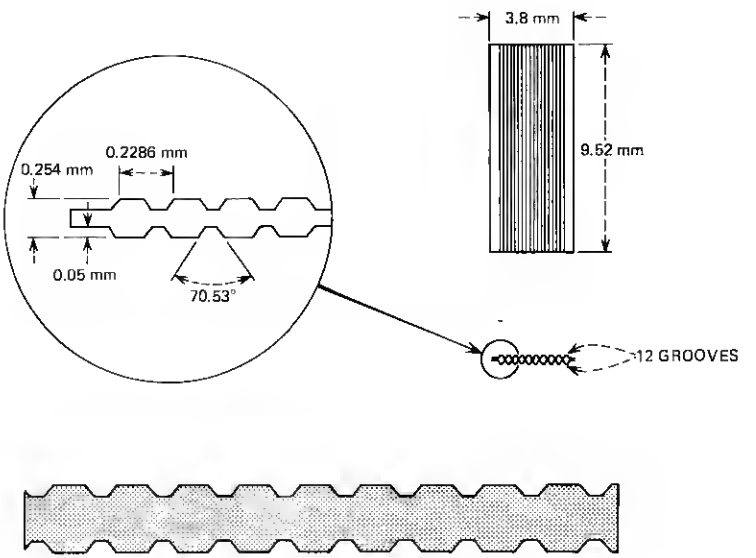

Fig. 4—Cross section of typical alignment chip with dimensions.

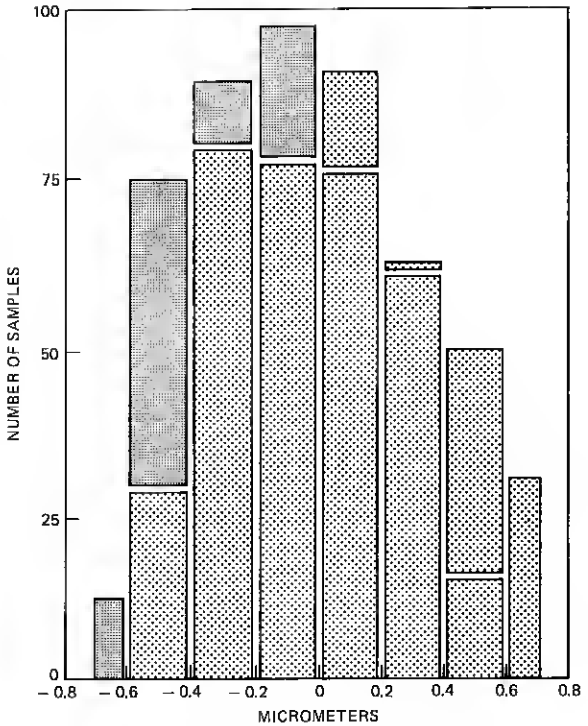

Fig. 5—Data on groove opening variations.

III. ALIGNMENT CHIP EVALUATION

A listing of variations that can cause splice loss in a multifiber connector in their present order of importance is as follows:

(*i*) Alignment chip thickness variations
(*ii*) Fiber diameter variations
(*iii*) Groove opening variations
(*iv*) Transverse misalignment of the top and bottom grooves
(*v*) Aperiodic grooves

Excluding fiber diameter variations, the remaining list must be controlled by alignment chip accuracy.

Measurements on the photomask features and the chip profile were made with the use of a Hewlett Packard model 5526A laser interferometer. The object whose features are to be measured is placed onto a traversing stage under the cross hair of a microscope. A reflecting cube attached to the stage monitors the movement of one of the two paths of the interferometer. This movement is compared to a fixed length of the second path with the changes displayed on a monitor. The repeatability

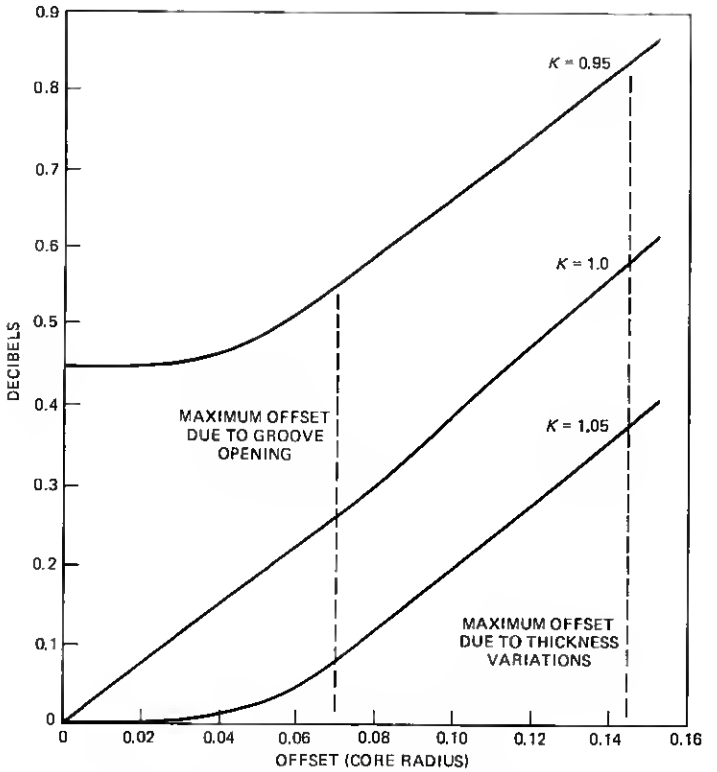

Fig. 6—Splice loss as a function of offset.

of the data was found to be 0.2 micrometer, limited chiefly by the vernier acuity of the eye.

Measurements on the photomask features indicate the required dimensions were well within the 1 micrometer stated accuracy for the masks with line-width variations not measurable across the mask face. Profile measurements on an etched silicon wafer indicate the groove periodicity of 228.6 micrometers was maintained within the measurement error. The transverse misalignment of the top and bottom grooves was held to 1 micrometer or less and the groove depth maintained at 50 micrometers. Variations of this type do not significantly add to the overall splice loss. The major contributors to array splice loss other than fiber diameter variations, was found to be chip thickness variations and groove opening variations.

The groove opening directly affects the vertical position of the optical fiber. The groove angle is constant but relatively steep with 1 unit of groove opening corresponding to 1.4 units of vertical drop in the optical fiber. The data on groove opening variations are shown in Fig. 5. These

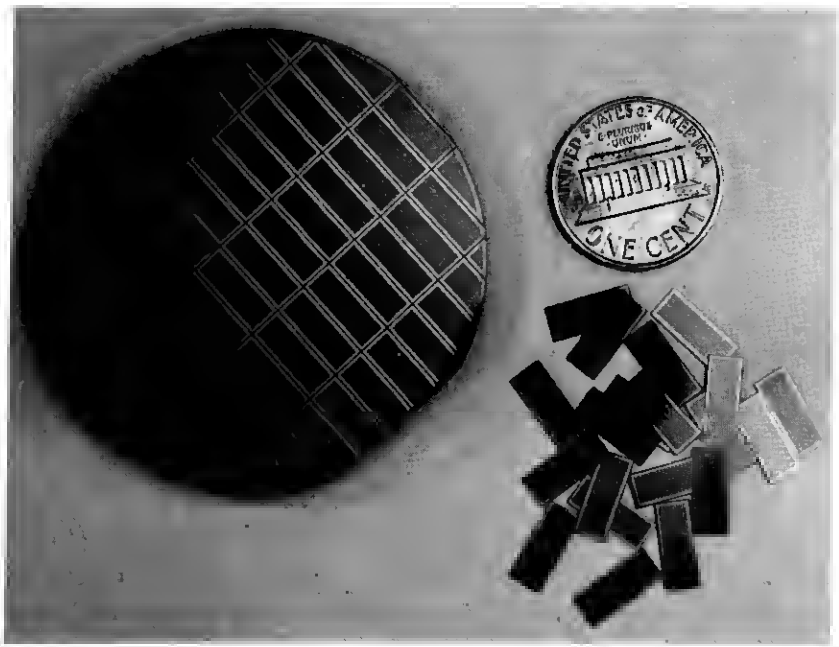

Fig. 7—Laser-scribed silicon wafer.

data were taken on both surfaces of one silicon wafer with the cross-hatched region being data from surface 1 superimposed onto data from surface 2. An overall shift in data of 0.2 micrometers can be observed when comparing the two surfaces. This shift was caused primarily by unequal exposure times. Maximum groove width variations were found to be ±0.7 micrometers with a standard deviation of 0.23 micrometers. The maximum difference in groove width of 1.4 micrometers would cause vertical positioning errors of the optical fibers of 1.96 micrometers for a worst-case situation. While this deviation does not exceed the 0.1 core radius offset, it does point to a need to minimize groove width variations, which are probably caused by variations in wafer thickness with Fresnel diffraction playing a part in undercutting at the areas where the wafer and photomask did not contact. Thickness variations are at present the largest potential contributor to splice loss with total variations of 4 micrometers encountered on some wafers.

IV. LOSS DUE TO TRANSVERSE OFFSETS

Splice loss as a function of offset for small offsets of parabolic index fibers is shown in Fig. 6.[3] K is the ratio of the radius of the receiving fiber to the radius of the transmitting fiber. The maximum offsets due to groove opening and thickness variations are displayed to indicate the

probable loss that could be expected in the worst-case situation. To avoid variations of this type an individual chip selection is required at present.

Splice loss data for 144-fiber array connectors using silicon alignment chips have been made with the results presented in a companion report by C. M. Miller.

V. SUMMARY AND CONCLUSION

A laser scribed silicon wafer is shown in Fig. 7. Each 5-cm diameter wafer yields 36 usable alignment chips 3.8 × 9.52 mm in size.

Assembled silicon array connectors have been fabricated with low splice loss. The silicon chips can be manufactured with submicrometer repeatability and accuracy. Improvements in chip thickness variations are anticipated which in turn should reduce the overall groove opening variations to a point where individual chip selection would not be required.

REFERENCES

1. C. M. Miller, "A Fiber-Optic Cable Connector," B.S.T.J., *54*, No. 9 (November 1975), pp. 1547–1555.
2. D. L. Bisbee, "Measurements of Loss to Offsets," B.S.T.J., *50*, No. 10 (December 1971), pp. 3159–3168.
3. C. M. Miller, "Loss vs. Transverse Offset for Parabolic Fiber Splices," B.S.T.J., *55*, No. 7 (September 1976), pp. 917–927.
4. L. P. Boivin, "Thin-Film Laser-to-Fiber Coupler," Appl. Opt., *13*, No. 2 (February 1974), pp. 391–395.
5. R. C. Kragness et al., "Etchant for Precision Etching of Semiconductors," Patent No. 3,506,509.